REMARKS

This paper is filed in response to the Office Action mailed on December 7, 2007. Claims 1-22 are pending in the application. Of these, Claims 1-14 are withdrawn from consideration as being directed to a non-elected invention. Claims 15-22 have been examined and stand rejected. Reconsideration of Claims 15-22 is respectfully requested.

The Rejection of Claims 15-18 and 20-22 Under 35 U.S.C. § 103(a)

Claims 15-18 and 20-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,370,013 (Iino et al.) in view of U.S. Patent Application Publication No. 2003/0128496 (Allen et al.).

In response thereto, Claim 15 has been amended to more particularly point out the claimed invention. Claim 15 is related to a printed circuit board with embedded capacitors. The printed circuit board includes a non-copper clad laminate having a plurality of inner via holes formed on its predetermined regions, wherein the via holes define a perimeter; a capacitor paste filled in the plurality of inner via holes formed on the non-copper clad laminate, wherein the capacitor paste fills the via holes to the perimeter of the via holes *and throughout the height of the via holes*; copper foil layers provided on both upper and lower surfaces of the capacitor paste and the copper clad laminate, the copper foil layers forming top electrodes, bottom electrodes, and signal circuit patterns, wherein a top electrode formed by a copper foil layer contacts the top of the capacitor paste at least over the area defined by the perimeter of the via hole and a bottom electrode formed by a copper foil layer contacts the bottom of the capacitor paste at least over the area defined by the perimeter of the via hole, *and wherein the signal circuit patterns formed by a copper foil layer are juxtaposed next to the top and bottom surfaces of the copper clad laminate at the height of the top and bottom electrodes of the capacitor* (see applicants' Figure 7f.); resin coated copper (RCC) layers laminated to the top electrodes, the bottom

LAW OFFICES OF
CHRISTENSEN O'CONNOR JOHNSON KINDNESS PLLC
1420 Fifth Avenue
Suite 2800
Seattle, Washington 98101
206.682.8100

electrodes, and the signal circuit patterns; predetermined outer via holes and through-holes formed in the resin coated copper layers; and plating layers plated in the inner walls of the outer via holes and the through-holes.

Iino et al. describes a capacitor 3 of Figure 2A has a capacitor body 3a that is formed by laminating ceramic dielectric layers 5. (Col. 6, lines 25-27.) The capacitor body 3a has four positive terminal electrodes 6a and four negative terminal electrodes 6b. In the capacitor 3 of Figure 2A, the negative terminal electrodes 6b are formed at the middle of each side of the capacitor 3 and the positive terminal electrodes 6a are formed at the corners of the capacitor 3. (Col. 6, lines 31-34.) Furthermore, Iino et al. describes a prepreg layer 1b made from fabric impregnated with a thermosetting resin juxtaposed at the bottom of the capacitor 3. (Col. 9, lines 23-24.) Accordingly, Iino et al. fails to teach or suggest various elements of Claim 15, including a capacitor paste that fills the inner via holes to the perimeter and throughout the height of the via hole. In Figure 1 of Iino et al., unlike Claim 15, the electrodes 6a and 6b partly fill the cavity 2; therefore, the capacitor does not fill the via hole (cavity) throughout the height. Iino et al. fails to disclose top and bottom electrodes on and below the capacitor paste that contact the capacitor paste at least over the area defined by the perimeter of the via hole. Iino et al. fails to disclose signal circuit patterns at the height of the top and bottom capacitor electrodes. Applicants' Figure 7f shows electrode 108a is at the same height of signal circuit 109 because they are both made from the same layer of copper foil. In Figure 1 of Iino et al., the electrodes 6a and 6b end at the boundary of the insulation layer 1a and prepreg layers 1b on top and 1b on bottom. The Examiner is asked to take note that there are no signal circuit patterns in the insulation layer 1a that are at the height of any of the electrodes 6a and 6b. Conductors 10 in the top prepreg layer 1b are *above* the electrodes 6a and 6b, while conductors 17 in the bottom prepreg layer 1b are *below* the electrodes 6a and 6b.

LAW OFFICES OF
CHRISTENSEN O'CONNOR JOHNSON KINDNESS PLLC
1420 Fifth Avenue
Suite 2800
Seattle, Washington 98101
206.682.8100

Allen et al. discloses a capacitor comprising a multilayer dielectric structure having bottom dielectric layer 20 and top dielectric layer 25 having a textured surface 30, a bottom conductive layer 35 in intimate contact with the surface of the bottom dielectric layer, and a top conductive layer 40 in intimate contact with the textured top dielectric structure surface. (¶[0053].) There is no hint of placing signal circuit patterns at the height of layer 35 and layer 40.

Accordingly, even considering the disclosures of both Iino et al. and Allen et al., one of ordinary skill could not derive the claimed printed circuit board with a capacitor, wherein the top and bottom electrodes of the capacitor are at the same height of the signal circuit patterns.

The teachings of the references are insufficient to render Claim 15 obvious. The printed circuit board and capacitor disclosed by Iino et al. cannot be modified as recited in Claim 15. First, modifying the capacitor of Iino et al. to have a first electrode on the top and a second electrode on the bottom would contradict with Iino et al.'s explicit teaching that a *plurality* of positive and negative electrodes performs better because the constitution [of the capacitor] decreases the inductance in comparison to a case of an ordinary capacitor having one positive electrode and one negative electrode. (See Col. 7, lines 14-22.) Second, Iino et al. discloses that the capacitor is manufactured independently of the printed circuit board, thus Iino et al. cannot achieve signal circuit patterns that are at the height of the top and bottom electrodes of the capacitor.

Specifically, Iino et al. discloses taking an uncured insulation sheet of a thermosetting resin, or a prepreg in uncured state made of woven fabric or nonwoven fabric of glass, fiber, or aramid fiber impregnated with a thermosetting resin. Then, a cavity 21 for housing the capacitor is formed by punching or the like in the prepreg 20. (Figure 4A.) Multiple insulation layers are provided that include via holes filled with a conductive paste. Each insulation sheet is provided

LAW OFFICES OF
CHRISTENSEN O'CONNOR JOHNSON KINDNESS PLLC
1420 Fifth Avenue
Suite 2800
Seattle, Washington 98101
206.682.8100

with a conductive layer formed on the surface of the insulation sheet. (Figure 4C.) Finally, the prepreg layer with one or more holes is provided with capacitors 26. The one or more insulation sheets are then assembled above and below the prepreg layer 20. Note that the circuit patterns are not at the height of the electrodes because the electrodes of the capacitor 26 only extend between the upper and lower surface of the individual capacitors. The assembly is then laminated by heating to a temperature that is high enough to harden the thermosetting resin included in the individual insulation sheets 30a, b, c, d, e prepreg and 20 (Figure 4D).

Even assuming that Allen et al. discloses a top and bottom electrode for a capacitor, the teachings of Iino et al. with the teachings of Allen et al. would still not have led one of ordinary skill to the printed circuit board of Claim 15 because Iino et al. specifically teaches against only having one positive electrode and one negative electrode. Furthermore, Iino et al. prepares the capacitor and then only inserts the assembled capacitor in the prepreg layer 20. Accordingly, it would not have been within the skill to make the claimed printed circuit board based on the teachings of Iino et al., even considering the teachings of Allen et al.

Accordingly, for the reasons discussed above, applicants submit that Claims 15-18 and 20-22 are not obvious. Accordingly, the withdrawal of the rejection is respectfully requested.

The Rejection of Claim 19 Under 35 U.S.C. § 103(a)

Claim 19 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Iino et al. in view of Allen et al., and further in view of U.S. Patent Application Publication No. 2004/0116919 (Heim et al.).

Heim et al. is merely cited for disclosing that capacitor material can be particles of $BaTiO_3$ in epoxy resin. Accordingly, Heim et al. does not disclose nor suggest the exact configuration of Claim 15. Furthermore, Claim 19 depends from Claim 15, which is submitted to be allowable.

Accordingly, the withdrawal of the rejection of Claim 19 is respectfully requested.

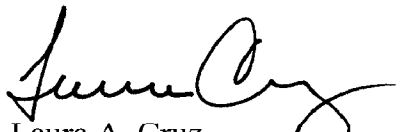
LAW OFFICES OF
CHRISTENSEN O'CONNOR JOHNSON KINDNESS PLLC
1420 Fifth Avenue
Suite 2800
Seattle, Washington 98101
206.682.8100

CONCLUSION

In view of the foregoing amendment and remarks, applicants submit that the application is in condition for allowance. If the Examiner has any further questions or comments, the Examiner is invited to contact the applicants' attorney at the number provided below.

Respectfully submitted,

CHRISTENSEN O'CONNOR
JOHNSON KINDNESS[PLLC]



Laura A. Cruz
Registration No. 46,649
Direct Dial No. 206.695.1725

LXC:aew